
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. RA043D2C3C2)

In the Application of:)
)
 FARMWALD ET AL.)
)
 Serial No: Continuation of 09/492,982)
)
 Filed: Herewith)
)
 Title: MEMORY DEVICE HAVING A VARIABLE)
 DATA OUTPUT LENGTH (As Amended))

Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Dear Sir:

Prior to the examination of the above-referenced application,
kindly amend the application as follows:

IN THE ABSTRACT:

Please delete the Abstract of the Disclosure and substitute the
attached Abstract of the Disclosure.

IN THE TITLE:

Please delete the title and substitute --MEMORY DEVICE HAVING A
VARIABLE DATA OUTPUT LENGTH--.

IN THE SPECIFICATION:

On page 1, line 8, insert --This application is a continuation of Application No. 09/492,982, filed January 27, 2000 (pending); which is a continuation of Application No. 09/252,997, filed February 19, 1999 (now U.S. Patent 6,034,918), which is a continuation of Application No. 09/196,199, filed on November 20, 1998 (now U.S. Patent 6,038,195), which is a continuation of Application No. 08/798,520, filed on February 10, 1997 (now U.S. Patent 5,841,580); which is a division of Application No. 08/448,657, filed May 24, 1995 (now U.S. Patent 5,638,334); which is a division of Application No. 08/222,646, filed on March 31, 1994 (now U.S. Patent 5,513,327); which is a continuation of Application No. 07/954,945, filed on September 30, 1992 (now U.S. Patent 5,319,755); which is a continuation of Application No. 07/510,898, filed on April 18, 1990 (now abandoned).--

On page 3, line 9, delete "micro-processor" and substitute --microprocessor--.

On page 6, line 1, delete "4,646,279" and substitute --4,646,270--.

On page 10, line 18, delete "Figure 7 shows" and substitute --Figures 7a and 7b show--.

On page 10, line 21, delete "Figure 8 shows" and substitute --Figures 8a and 8b show--.

On page 11, line 14, insert:

--Figure 16 is a block diagram representation of a set of internal registers within each device illustrated in Figure 2.--

On page 14, line 3, replace "Each" with --With reference to Figure 16, each--.

On page 14, line 4, after "registers" insert --170--.

On page 14, line 5, after the first occurrence of "register" insert --171--.

On page 14, line 5, after the second occurrence of "register" insert --174--.

On page 14, line 6, after the first occurrence of "register" insert --175--.

On page 14, line 8, after "registers" insert --172--.

On page 14, line 10, after "registers" insert --173--.

On page 14, line 17, after "register" insert --171--.

On page 14, line 20, after the first occurrence of "registers" insert --173--.

On page 14, line 20, after the second occurrence of "registers" insert --175--.

On page 14, line 20, after the third occurrence of "registers" insert --172--.

On page 14, line 22, after "registers" insert --173--.

On page 21, line 15, after "registers" insert --173--.

On page 34, line 4, after "devices" insert --do--.

On page 35, line 25, after "registers" insert --170--.

On page 36, line 10, after "registers" insert --173--.

On page 36, line 15, after "register" insert --171--.

On page 36, line 12, after "registers" insert --172--.

On page 38, line 25, after "register" insert --173--.

On page 39, line 6, after "register" insert --173--.

On page 41, line 1, delete "or" and substitute -- or--.

On page 45, line 17, delete "Fig. 7" and substitute --Figures 7a and 7b--.

On page 47, line 2, delete "Figure 8" and substitute --Figure 8a--.

On page 47, line 5, delete "from left to right" and substitute --from right to left--.

On page 47, line 8, delete "right" and substitute --left--.

On page 47, line 9, delete the first "left" and substitute --right--.

On page 49, line 22, delete "primay" and substitute --primary--.

On page 54, line 13, delete "70" and substitute --69--.

On page 56, line 2, delete "Figure11" and substitute --Figure 11--.

On page 58, line 22, after "clocks" insert --73 and 74, respectively--.

On page 60, line 10, after "147" insert --A, B-.

IN THE CLAIMS:

Kindly cancel claims 1-150, without prejudice.

Kindly add the following claims:

1 --151. A method of operation of a synchronous memory device,
2 wherein the memory device includes an array of memory cells, the method
3 of operation of the memory device comprises:

4 receiving an external clock signal;

5 receiving block size information, wherein the block size
6 information defines an amount of data to be output by the memory device
7 in response to a read request;

8 receiving a first read request synchronously with respect to a
9 rising edge transition of the external clock signal; and

10 outputting the amount of data, in response to the first read
11 request, the amount of data corresponding to the block size
12 information.

1 152. The method of claim 151 wherein the block size information
2 defines an amount of data to be input by the memory device in response
3 to a write request, the method further including:

4 receiving a first write request synchronously with respect to a
5 transition of the external clock signal; and

6 inputting the amount of data, in response to the first write
7 request, the amount of data corresponding to the block size
8 information.

1 153. The method of claim 152 wherein a first portion of data is
2 sampled, in response to the first write request, after a delay time
3 transpires.

1 154. The method of claim 151 wherein the amount of data is output
2 synchronously with respect to the external clock signal.

1 155. The method of claim 154 wherein a first portion of data is
2 output synchronously with respect to a rising edge transition of the
3 external clock signal and a second portion of data is output
4 synchronously with respect to a falling edge transition of the external
5 clock signal.

1 156. The method of claim 151 wherein the first read request is
2 specified by an operation code.

1 157. The method of claim 156 wherein the operation code includes
2 precharge information.

1 158. The method of claim 156 wherein the operation code is
2 included in a request packet.

1 159. The method of claim 158 wherein the block size information
2 and the operation code are both included in the same request packet.

1 160. The method of claim 158 wherein the request packet includes
2 address information.

1 161. The method of claim 151 wherein the block size information
2 is sampled synchronously with respect to the external clock signal.

1 162. The method of claim 151 further including:
2 receiving a code which is representative of a number of clock
3 cycles of the external clock signal to transpire before the memory
4 device responds to the first read request; and
5 storing the code in a register.

1 163. The method of claim 162 wherein the memory device outputs a
2 first portion of data after the number of clock cycles of the external
3 clock signal transpire.

1 164. The method of claim 151 wherein the block size information
2 is a binary code.

1 165. A method of controlling a synchronous memory device by a
2 controller, wherein the memory device includes an array of memory
3 cells, the method of controlling the memory device comprises:

4 providing block size information to the memory device,
5 synchronously with respect to an external clock signal, wherein the
6 block size information defines an amount of data to be output by the
7 memory device in response to a read request; and

8 issuing a first read request to the memory device, wherein the
9 memory device receives the first read request synchronously with
10 respect to a transition of the external clock signal.

1 166. The method of claim 165 further including receiving the
2 amount of data from the memory device.

1 167. The method of claim 165 further including providing a code
2 to the memory device, wherein the code is representative of a number
3 of clock cycles of the external clock signal to transpire before the
4 memory device responds to the first read request.

1 168. The method of claim 167 further including providing a set
2 register request to the memory device, wherein the memory device stores
3 the code in a register in response to the set register request.

1 169. The method of claim 165 wherein the first read request is
2 specified by an operation code.

1 170. The method of claim 169 wherein the operation code includes
2 precharge information.

1 171. The method of claim 169 wherein the operation code is
2 included in a request packet.

1 172. The method of claim 171 wherein the block size information
2 is included in a request packet.

3 173. The method of claim 171 wherein the block size information
4 and the operation code are both included in the same request packet.

5 174. The method of claim 171 wherein the request packet further
6 includes address information.

1 175. The method of claim 165 wherein the block size information
2 is a binary code.

1 176. A synchronous semiconductor memory device having at least one
2 memory section including a plurality of memory cells, the memory device
3 comprising:

4 clock receiver circuitry to receive an external clock signal;
5 input receiver circuitry to receive block size information
6 synchronously with respect to the external clock signal, wherein the
7 block size information defines an amount of data to be output by the
8 memory device in response to a read request; and

9 a plurality of output drivers to output the amount of data
10 corresponding to the block size information, wherein the first amount
11 of data is output in response to the read request.

1 177. The memory device of claim 176 wherein the amount of data is
2 output synchronously with respect to the external clock signal.

1 178. The memory device of claim 177 wherein a first portion of
2 data is output synchronously with respect to a rising edge transition
3 of the external clock signal and a second portion of data is output
4 synchronously with respect to a falling edge transition of the external
5 clock signal.

1 179. The memory device of claim 176 wherein the first read request
2 is specified by an operation code.

1 180. The memory device of claim 179 wherein the operation code is
2 included in a request packet.

1 181. The memory device of claim 180 wherein the block size
2 information is included in a request packet.

1 182. The memory device of claim 181 wherein the block size
2 information and the operation code are included in the same request
3 packet.

1 183. The memory device of claim 179 wherein the operation code
2 includes precharge information.

1 184. The memory device of claim 176 further including a
2 programmable register to store a value which is representative of a
3 number of clock cycles of the external clock signal to transpire before
4 the memory device responds to a read request.

1 185. The memory device of claim 176 wherein the block size
2 information defines an amount of data to be input in response to a
3 write request.

1 186. The memory device of claim 185 wherein the input receiver
2 circuitry samples a first portion of the amount of data in response to
3 the write request.

1 187. The memory device of claim 186 wherein the input receiver
2 circuitry samples the first portion of the amount of data, in response
3 to the write request, after a delay time transpires.

1 188. The memory device of claim 176 further including delay lock
2 loop circuitry coupled to the clock receiver circuitry to generate an
3 internal clock signal, wherein the plurality of output drivers output
4 data in response to the internal clock signal.

1 189. The method of claim 176 wherein the first block size
2 information is a binary code.--

REMARKS

This Preliminary Amendment seeks to place this application in condition for allowance. This application is a continuation of Application No. 09/492,982 which is a continuation of Application No. 09/252,997 (now U.S. Patent 6,034,918). Application Serial No. 09/492,982 is pending.

Applicants request priority to Application Serial No. 07/510,898, filed April 18, 1990, now abandoned. Applicants request such priority through Application No. 09/492,982, filed January 27, 2000 (pending); which is a continuation of Application No. 09/252,997 (now U.S. Patent 6,034,918), which is a continuation of Application No. 09/196,199, filed on November 20, 1998 (now U.S. Patent 6,038,195), which is a continuation of Application No. 08/798,520, filed on February 10, 1997 (now U.S. Patent 5,841,580); which is a division of Application No.

08/448,657, filed May 24, 1995 (now U.S. Patent 5,638,334); which is a division of Application No. 08/222,646, filed on March 31, 1994 (now U.S. Patent 5,513,327); which is a continuation of Application No. 07/954,945, filed on September 30, 1992 (now U.S. Patent 5,319,755); which is a continuation of Application No. 07/510,898, filed on April 18, 1990 (now abandoned).

Accordingly, Applicants claim the benefit of the filing date of Application Serial No. 07/510,898 -- i.e., April 18, 1990. The specification has been amended to identify the continuation or related U.S. application data identified above. No new matter has been added.

In this continuation application, Applicants present new claims which set forth novel and unobvious features of Applicants' invention. Applicants submit new claims 151-189 to more fully protect the instant invention. No new matter has been added.

The newly submitted claims are believed to be fully supported by the specification -- see, for example, Figures 2, 4, and 10-13; page 14, line 3 to page 16, line 7; page 20, line 14 to page 21, line 20; page 22, line 11 to page 25, line 8; page 27, line 1 to page 28, line 20; page 46, line 19 to page 48, line 17; page 53, line 23 to page 59, line 2; page 71, line 20 to page 72, line 21; page 73, lines 20 to page 74, line 31; and page 115, lines 10-22.

Applicants have also amended the specification to correct obvious spelling, typographical and grammatical errors. No new matter has been added.

In addition, a new Abstract of the Disclosure is attached hereto. No new matter has been added.

Finally, accompanying this Preliminary Amendment is a Request to Approve Drawing Changes. Applicants have amended the drawings to show every feature of the invention specified in the claims. To that end, Applicants submit herewith new Figure 16, and amended Figure 10. A copy of Applicants Request to Approve Drawing Changes is attached.

New Figure 16 is added to illustrate, among other things, access-time register(s) 173. Figure 16 illustrates one embodiment of the internal registers within each device illustrated in Figure 2. Support may be found in the specification at page 14, lines 3-21 and page 53 lines 4-21. No new matter has been added.

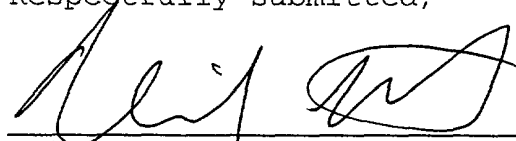
Applicants seek to amend Figure 10 to more fully reflect the discussion in the specification, in particular, page 55, lines 12-16 and page 58, lines 13-23. The proposed changes are indicated in red. No new matter has been added. Applicants respectfully request that the Examiner approve the proposed changes to Figure 10. A new Figure 10 which incorporates the changes is also attached to the Request.

CONCLUSION

Applicants request entry of the foregoing amendment prior to examination of this application. Applicants submit that all of the claims present patentable subject matter. Accordingly, Applicants respectfully request allowance of all of the claims.

Respectfully submitted,

Date: Feb. 7, 2001


Neil A. Steinberg
Reg. No. 34,735
650-947-5325

	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415	2416	2417	2418	2419	2420	2421	2422	2
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A synchronous memory device and methods of operation and controlling such a device. The method of controlling the memory device includes providing block size information to the memory device, synchronously with respect to an external clock signal, wherein the block size information defines an amount of data to be output by the memory device in response to a read request. The method further includes issuing a first read request to the memory device, wherein the memory device receives the first read request synchronously with respect to a transition of the external clock signal.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. RA043D2C3C2)

In the Application of:

FARMWALD ET AL.

Serial No: Continuation of 09/492,982

Filed: Herewith

Title: MEMORY DEVICE HAVING A VARIABLE
DATA OUTPUT LENGTH (As Amended)

Assistant Commissioner for Patents
Washington, DC 20231

REQUEST TO APPROVE DRAWING CHANGES

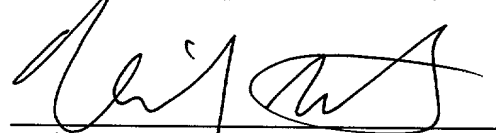
Dear Sir:

Attached hereto is new Figure 16. Figure 16 illustrates the internal registers which reside in each device illustrated in Figure 2. This embodiment is described in the specification at page 14, lines 3-21 and page 53 lines 4-21. No new matter has been added.

Applicants seek to amend Figure 10 to more fully reflect the discussion in the specification, specifically, page 55, line 12-16 and page 58, lines 13-23. Also attached, is a photocopy of Figure 10 with the proposed changes indicated in red. No new matter has been added.

Applicants respectfully request that the proposed new Figure 16 be approved by the Examiner. Applicants also respectfully request approval of the proposed changes to Figure 10. A new Figure 10 which incorporates the changes is also attached hereto.

Respectfully submitted,



Neil A. Steinberg
Reg. No. 34,735
650-947-5325

Date: Feb 7, 2001

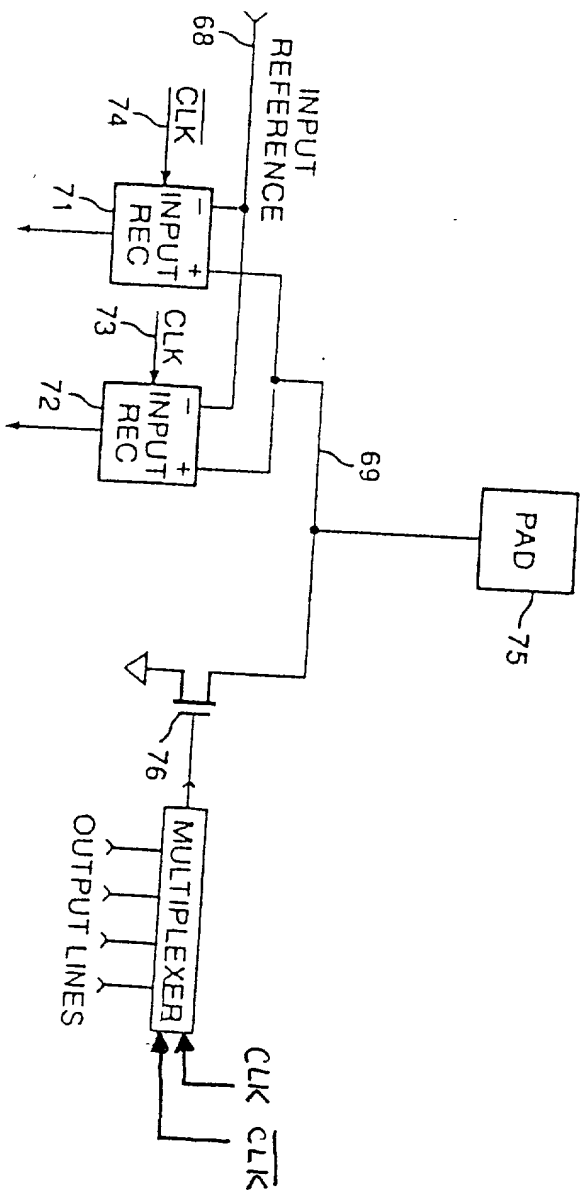


FIG. 10

FIG. 10 is a block diagram of a circuit 100. The circuit 100 includes a first input register 72, a second input register 73, a multiplexer 76, and a PAD 75. The first input register 72 and the second input register 73 are connected in a differential configuration. The first input register 72 has a non-inverting input (+) and an inverting input (-). The second input register 73 has a non-inverting input (+) and an inverting input (-). The inverting input of the first input register 72 is connected to the non-inverting input of the second input register 73, and the non-inverting input of the first input register 72 is connected to the inverting input of the second input register 73. Both input registers 72 and 73 are clocked by a common CLK signal 74. A REFERENCE signal 68 is applied to the inverting input of the first input register 72. The output of the first input register 72 is connected to a node 69. The node 69 is also connected to the PAD 75 and the gate of a PMOS transistor 76. The PMOS transistor 76 is connected to the multiplexer 76. The multiplexer 76 has multiple OUTPUT LINES and is clocked by a CLK signal.

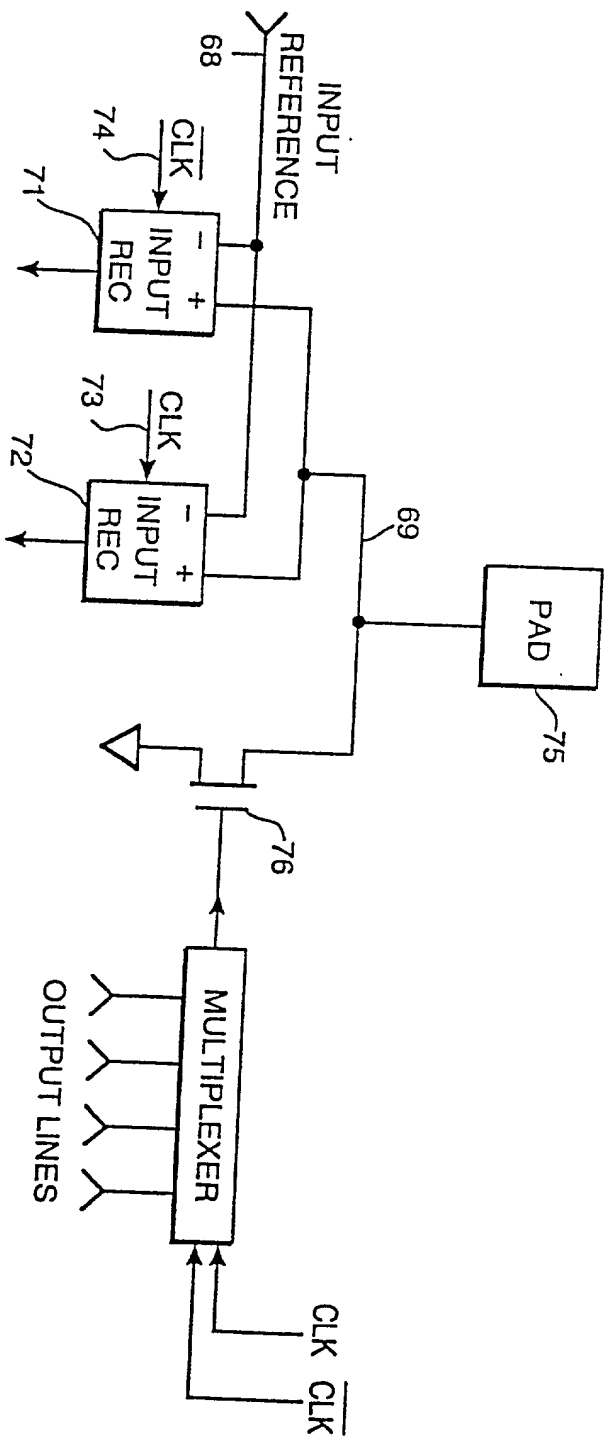


FIG. 10

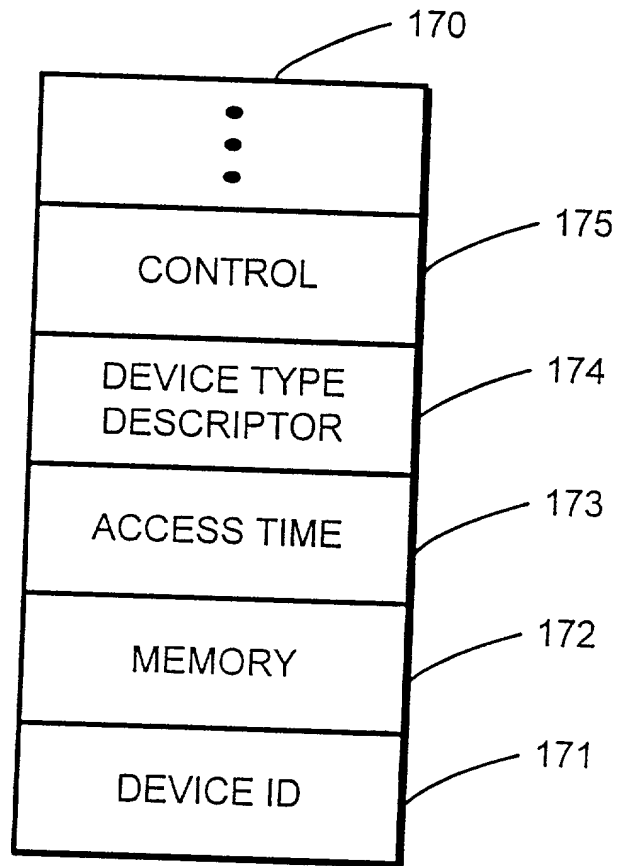


FIG. 16